Lecture Plan

Name of Subject: DIGITAL SYSTEM DESIGN (E-302)

Class: B.Tech (EIC)

Semester: 6th

S.No.	UNIT	TOPICS COVERED	NUMBER OF LECTURES
1	Unit-1	Introduction to HDL: Design flow, Design methodologies, Capabilities, Hardware abstraction, Model analysis	03
2	Unit-1	Basic HDL elements—Identifiers, data objects, data classes, data types, Operators	04
3	Unit-2	Types of Modeling: Behavioral Modeling—Entity declaration, Architecture body. Various Sequential statements and constructs, Multiple processors, Postponed processes	05
4	Unit-2	Dataflow Modeling—Concurrent signal assignment statements, delta delay model, multiple drivers, block statement, concurrent assertion statement.	04
5	Unit-2	Structural Modeling—Component declaration, component instantiation, resolving signal values.	03
6	Unit-3	Combinational Circuit Design: VHDL Models and simulation of combinational circuits such as Multiplexers, Demultiplexers, encoders, decoders, code converters, comparators, implementation of Boolean functions etc	06
7	Unit-4	Supporting Constructs: Generics, Configuration, subprogram overloading, operator overloading. Packet declaration, package body, design libraries, visibility.	04
8	Unit-4	Introduction to test bench, Subprograms: Application of functions and procedures.	04
9	Unit -5	Sequential Circuits Design: VHDL Models and Simulation of Sequential circuits such as flip flops, Shift registers, Counters etc.	05

10	Unit-6	Programmable Logic Devices: ROM, PLA, PAL, GAL, CPLD and FPGA, Designing using ROM, PLA and PAL	03