

Nitin Sachdeva

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Educational Qualification

Education	Board/ University	Year of passing	Marks / Grade
M-Tech.(VLSI Design & CAD)	Thapar Institute of Engineering & Technology, Deemed University, Patiala	2005	C.G.P.A. – 7.49
B-Tech (Electronics & Communication Engg.)	Punjab Technical University, Jalandhar	2003	71%
Diploma (Electronics & Communication Engg.)	Punjab State Board of Tech. Edu. & Industrial Training, Chandigarh	2000	67 %
Matric	Punjab School Education Board, S.A.S Nagar	1997	73 %

Technical Skills**Languages**

VHDL, C

OS

MS-DOS, Windows 9x/2000, Linux

Applications

Tanner EDA Tools, Modelsim, Matlab, Xilinx

Foundation Series ISE-6, SILVACO

MTech. Thesis Work

“Design & Implementation of Asynchronous Transfer Mode (ATM) switch on FPGA”. In this, a high speed 4 x 4 ATM switch is designed using VHDL language. The simulation, synthesis and implementation of the design are performed using **Xilinx Foundation Series ISE-6** having simulation software **Modelsim 5.5e** and tested on **Xilinx Spartan2 xc2s30-5-pq208** Field programmable Logic device.

Industrial Trainings

- **Six Months Industrial Training at PUNCOM, Mohali**

I have worked on Digital Power line Carrier Communication Project. Power Line carrier is used in almost all the countries of the world to transfer information via high voltage transmission lines and has become important equipment for the management and safety of electrical power systems. The range of frequencies suitable for PLCC extends from about 30 KHz to 500 kHz. In PLCC the voice signal is modulated on carrier frequency and is transmitted on a power lines.

- **Six Weeks Training at Bharat Sanchar Nigam Limited, Sangrur**

In CDOT Exchange

Publications in International/National Conferences

1. "AN EFFICIENT SIMULATION OF D-FLIP-FLOP USING THE GDI TECHNIQUE" at International Conference on Extropianism: Towards Convergence of Human Values and Technology 2013 organized at Ansal University, Gurgaon on 18-19 January, 2013
2. Meenakshi Yadav,Nitin Sachdeva"Design and Implementation of Folded Cascode OTA" in NCNPECC 2012
3. Jitender Kumar, Munish Vashishath,Nitin Sachdeva"Leakage Power Reduction in CMOS Logic Circuits by Transistor Stacking Technique" in NCNPECC,2012
4. "Comparative study of CMOS inverter using different Logic structures" ISTE Sponsored workshop on Nanotechnology and Embedded Systems WNTES 2012 held at YMCA UST , dated 23rd July to 3rd August,2012

Publications in International Journals

1. "Leakage Reduction in various Logic circuits using VTCMOS technique" Nitin Sachdeva, Tarun Sachdeva, Dr. Munish Vashishath, Nisha Kumari"International Journal of advanced & innovative research IJAIR- Volume 2 Issue 2,2013
2. "VTCMOS Leakage Reduction in various logic circuits" Tarun Sachdeva, Nitin Sachdeva, , Dr. S.K Aggarwal, Nisha Kumari"International Journal of advanced & innovative research IJAIR- Volume 2 Issue 3,2013
3. Nitin Sachdeva, Neeraj Julka" Effect of Temperature Fluctuations on MOSFET Characteristics" International Journal of Electronics and Communication Technology (IJECT) Vol. 2 Issue 1 March, 2011
4. Nitin Sachdeva "Design of Second-Order Sigma-Delta Modulator using CMOS Technology" International Journal of "Computer Science and Communication (IJCS) Vol. 2, Issue-I March,2011
5. "Design and Analysis of carry look ahead adder using CMOS technique"IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 9, Issue 2, Ver. VII (Mar - Apr. 2014), PP 92-95.
6. "Implementation and study of quaternary multiplexer using universal set of gates" International Journal of Engineering Research and General Science Volume 3, Issue 3, May-June, 2015 ISSN 2091-2730,2015
7. "Analysis and Design of a Two Stage CMOS OP-AMP with 180nm using Miller Compensation Technique" International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169 Volume: 3 Issue: 4 2255 – 2260,2015

Short Term Courses

1. "Quality Assurance in Teaching Learning process" at Bharati Vidyapeeth Institute of Management & Research,New Delhi(14/5/2012-27/05/2012)
2. "Applications of Advanced Computing Technologies:The Emerging Research Trends" at Ambedkar Institute of Technology"(2/1/2012-14/1/2012)
3. "Embedded Systems & Nanotechnology" WNTES-2012 (23rd July,2012 to 3rd August,2012), YMCA University of science & technology, Faridabad
4. Application of Artificial Intelligence Tools in Power System" from 19th June 2012 to 25th June 2012 in Electrical Department, YMCAUST, Faridabad

5. "Digital Signal Processing and its applications" at Indira Gandhi institute of Technology, Delhi(20-06-2011 to 24-06-2011)
6. "Design and analysis of Engineering Experiments" at Gautam Buddha University, Greater Noida(04/07/2011 to 08/07/2011)
7. "Matlab Based Advanced Digital Signal processing"at NITTR, chd(23/5/2011-27/5/2011)
8. "Taguchi:A Statistical Technique" at Gautam Buddha University, Greater Noida (26/12/2011-30/12/2011)
9. "New Trends in Electronics and Communication" ISTE Sponsored STC at YMCAUST, Faridabad ("17th to 21st August), 2015

Work Experience

1. Worked as a Lecturer in Electronics & Communication Department in CITM, Faridabad.
2. Worked as a Sr.Lecturer in Electronics & Communication Department in ITM, Gurgaon.
3. Worked as a Lecturer in Electronics & Communication Department in Sant Longowal Institute of Engineering & Technology, Longowal (Sangrur, Punjab)

Achievements

- Roll of Honour by Chief Minister, Punjab - Deptt. Of Sports & Punjab Olympic Association (Softball)
- Winner - National Softball Championship, Kurukshetra
- Third Position (Softball) -XII National School Games Softball Championship, Jalandhar
- Third Position (Softball) - 42nd National School Games 1996, Delhi
- Colour Certificate (Badminton) - Punjab Technical Institutions Sports, Jalandhar

Personal Details

Husband's Name	Mr. Tarun Sachdeva
Date of Birth	July 24, 1981
Address	#2 L / 58, N.I.T, Faridabad (Haryana)
Gender	Female
Marital Status	Married
Nationality	Indian.
Language Known	Hindi, English, Punjabi.