CURRICULUM VITAE

NISHA YADAV

Masters of Technology

VLSI Design
Batch of 2014,
YMCA University of Science and Technology, Faridabad
India.

Permanent Address
V.P.O.- Jaitpur Shekhpur,
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Personal Data
Date of Birth : 22-03-1990
Sex : Female
Nationality : Indian
Languages known: English, Hindi

Hobbies
- *Surfing net*
- *Playing chess*
- *Painting*

Technical Interest
- Tanner EDA Tools
- MATLAB
- Xillinx and Modelsim
- Analog IC design/CAD with particular emphasis in high speed low-power electronics.

Achievements:

- **Qualified NET for both JRF and AP.**
- **Qualified GATE 2012, 2014, 2015 and 2016.**
- Received award of **Most Active Member** at MRU.
- Received Dean Certificate of Merit during all the four semesters of M.Tech
- Participated in Drontech.
- Member of IETE.

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Objective

To be part of a progressive organization where I can learn, how to incubate an elegant idea, formulate it succinctly and passionately strive to reach the goal with scientific integrity.

Academic Qualifications

M.Tech (2014)	**YMCA**	**: 9.2/10**
B.Tech (2011)	**MDU**	**: 78.3%**
Sr. Secondary Marks (2007)	**CBSE**	**: 81.3%**
Secondary Marks (2005)	**CBSE**	**: 71.0%**

Experience

- Working as an Assistant Prof. at **YMCA University of Science and Technology** from Feb. 14, 2017 till present.
- Worked as an Assistant Prof. at **Manav Rachna University** from July 14, 2014 to Feb. 13, 2017.
- Worked as a TPO Coordinator at **Manav Rachna University** from July , 2014 to Feb., 2017.

Projects & Training

- **M.Tech Thesis:** Design and Analysis of Power Efficient 9T Adiabatic SRAM Cell.
- **B.Tech Project**: Under Water Laser Communication System.
- **B.Tech Internship**: PC to PC LASER Communication System at Laser Science and Development Centre (LASTEC), Defence Research and Development Organization (DRDO), New Delhi, during the period of six weeks in June- August 2010.

Publications

Papers Published:

- Nisha Yadav and Pardeep, "A Review: Process Challenges and Performance Improvement of FinFET", International Journal of Innovative Research in Computer and Communication Engineering, Vol. 4, Special Issue 4, August 2016.
- Amita, Nisha Yadav and Pardeep ,"Design And Analysis Of Vedic Multiplier Using Microwind", *International journal of Electrical and Electronics Engineers, Vol. No. 8,Issue 01, Jan-June 2016.*
- Nisha Yadav, Sunil Jadav and Pardeep, "Design and Analysis of Power Efficient 9T Adiabatic SRAM Cell" ,*International journal of VLSI and Embedded Systems-IJVES,* Vol 06, Article 09641, October 2015.
- Pardeep , Nisha and Abhishek Agal, "Design and Analysis of Low-Power Area Efficient Comparators", *International journal of Electrical and Electronics Engineers,* Vol. 7, Issue-02, July-December 2015.
- Nisha Yadav and Sunil Jadav, "Efficient Energy Recovery in 9T Adiabatic SRAM Cell using Body Bias" ,*International journal of VLSI and Embedded Systems-IJVES,* Vol 05, Article 03244, March 2014.

Conference

- Nisha Yadav, Abhishek Agal and Pardeep," Design of a New Single Ended, Separated Read Port, Asymmetric 7T SRAM Cell" in Proceedings of the 11th INDIACom; INDIACom-2017; IEEE Conference ID: 40353.

Courses and workshops

- Attended one week STC on "FPGA Programming" at NITTTR, Chandigarh from Feb. 1,2016 to Feb. 5, 2016.

Declaration

I hereby declare that information provided by me is true to best of my knowledge.

(Nisha Yadav)