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An Approach for Digital Controlled Oscillator Optimization Using Meta-Heuristic Algorithms

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Abstract: Phase Locked Loop (PLL) has greatly revolutionised in communications and control systems since its introduction in 1980. PLL has become particularly significant since Integrated Circuit (IC) design techniques were used in its creation. The performance of PLL has been always improving since its introduction. In the present scenario, All Digital Phase Locked Loop (ADPLL) is extensively utilised among all PLL's in many different areas, such as digital communication networks, biomedical, signal processing, and the Internet of Things (IoT). This paper explains the concept and functioning of an ADPLL. It offers a succinct summary of the fundamental ADPLL principle, which is useful for control and network communication technologies. It also describes the basic architecture of the Digital Control Oscillator (DCO) as it is described in published works. DCO plays an important role in the power consumption of the ADPLL. In this paper, different optimization techniques which falls mainly into two categories: accurate procedures and approximate ones have been explored. Among different optimization techniques, in recent decades, researchers have suggested that nature is an excellent source for solutions to difficult problems. This paper explores different strategies of nature – inspired optimization algorithms that can be used for DCO parameter optimization. The optimal solution to a challenging problem has been found using an optimization strategy by defining the constraints' values and maximising or reducing the objective function. Furthermore, the framework for optimising DCO parameters using nature inspired optimization algorithm has been presented in this paper.
Keywords: *Phase locked loop, Phase frequency detector, All digital phase locked loop, Metaheuristic optimization algorithms, Digital controlled oscillator.*

1. Introduction

PLLs were widely utilized in reliable distance and speed measuring, demodulation, frequency generation and other applications. All of this is due to its excellent narrowband processing capability and its potential for accurate frequency management. There are presently two commonly used PLLs: analogue PLL and the All Digital Phase Locked Loop (ADPLL) (Pan & Huang, 2007). The disadvantages of the analogue PLL are sensitivity to drift temperatures and voltage variations. But considering that the Digital Phase Locked Loop (DPLL) has no such drawbacks, it offers different advantages, such as stability analysis, consistency and easy tweaking. PLL already used in visual representation, modulation demodulation, synthesis of frequency, FM stereophone decoding and other applications. PLL looks to have become a basic part of many forms of network equipment, due to its widely dispersed applications in communications, radar, measurement, automation control and other areas (Junzhao & Caim, 2006). Digital signals must be utilized for phase locked signal processing as electrical technology moves towards digitalization (Best, 2007). Simultaneous synchronization of electronics oscillators was characterized in 1923. The

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oldest known research into the so called PLL was carried out in 1932 when British investigators developed the Homodyne or direct conversion transmitter as an alternative to the Superheterodyne receiver by Edwin Armstrong (Appleton, 1922). A local oscillator that could adapt to the specified input frequency and multiply by the input voltage was used in the synchrodyne homodyne system. The resultant output signal included the information about the original modulation. An alternate superheterodynamic circuit was designed that would need less tuned circuits. The oscillator was given a standalone correction signal to keep it at the intended signal while at the same frequency. In 1932, in L'Onde Électrique, Henri dé Bellescize wrote a research article outlining the process (Bellescize, 1932).

In the early 1930s, it moved from its early examination to a state-of-the-art IC to synchronize horizontal and vertical TV scans. The primary PLL ICs were initially presented about 1965; they consisted exclusively of analogue components. Signetics released several monolithic Integrated Circuits (ICs) in 1969, namely the NE565 which included extensive PLL systems on a semiconductor, leading to an increase in the application (Grebene & Camenzind, 1969). A few years later, RCA created a "CD4046," which immediately became a famous IC. It is currently employed in a range of applications. Latest development in IC design methodologies have contributed to the growth of more cost effective and reliable high performance PLLs. A comprehensive PLL circuit can then be integrated on a single chip as part of a bigger circuit.

ADPLLs are more appealing as they offer greater flexibility and adaptability than PLL's (Chiang & Chen, 1999; Goldberg, 1999; Retdian, Takagi, & Fujii, 2002). Because the ADPLL must allow quick entry and exit from energy management strategies, lock duration is especially relevant for mobile and portable applications. Fast frequency synchronization, full digitalization, and exceptional stability are all features of ADPLLs. It utilizes different digitally controlled oscillator (DCO) techniques to achieve different objectives of ADPLLs revealed in. There are some of the objectives of the ADPLL:

1. Lock Time should be fast
2. Wide Operating Range
3. Area should be reduced
4. Less power consumption

The Control Unit/ Digital Loop Filter (DLF) and the oscillator are traditionally designed as analogue IP Blocks that are responsive to process fluctuations. Each new manufacturing technique necessitates the modification of these components. ADPLLs have gained popularity in recent years because of noise couplings and power distribution noise effects, as they lessen integration challenges in a digital loud environment. Two issues must be carefully examined when designing an ADPLL: first is how to create a high resolution and wide range DCO. As a result, a selected inverter chain offers a wide range of operations. A circle oscillator with parallel coupled tristate inverters can be used to obtain great resolution. Furthermore, incorporating buskeeper components is a viable option. The second issue is how the frequency and phase convergence of the both signals can be accelerated. PLLs in a range of applications are now widely used. For instance, a clock generator chip for high speed clock signal generation, recovery of clock, chip synchronization and chip jitter and phasing noise. The PLL comprises usually of analogue components such as a required charge pumping and a voltage controlled oscillator (VCO). The leakage phenomenon in modern CMOS methods is getting increasingly serious. The effort and complexity of creating an analogue PLL are therefore increasing with technology (Chung & Lee, 2003). The ADPLL has several improve-

ments over analogue PLL. In a wide range of procedures, ADPLLs provide noise immunity, testability, reconfiguration, stability and portability. They can also reduce the amount of time that the system needs to react. The analogue PLL suffer from the decreased supply voltage and increasing gate leakage when CMOS scales in nanometers. In addition, the complexity and sophistication of analogue PLL are increasing as technology improves (Hwang, Lee, Lee, & Kim, 2000; Hsu, Wang, & Lee, 2001). The ADPLL reduces susceptibility to variations in the voltage, temperature, area and power consumption of the process (Dunning, Garcia, Lundberg, & Nuckolls, 1995). ADPLL is based on the DCO and the DCO design has improved in the past year following the different standards required by ADPLL. The noise sensitivity of the provider, DCO resolution, frequencies step size, range of frequencies, and supply voltage must all be taken into consideration during the construction of a DCO. In the paper, section 2 describes the block level structure of ADPLL and its working, section 3 discusses the different types of DCO available in literature, section 4 explains the different metaheuristic optimization techniques available and section 5 describes the framework of DCO parameter optimization using metaheuristic optimization techniques.

2. Structure of ADPLL

Analog or digital circuits can be used to build PLL. The underlying structure of PLL shown in Figure 1 is the same in both implementations. There are four main elements in both analogue and digital PLL circuits:

- Phase detector or Phase and Frequency Detector,
- Control Unit,
- Oscillator of variable frequency, and
- Feedback path that could incorporate a splitter of frequencies.

These blocks are implemented moreover in analog form otherwise in digital form depending upon the type of PLL. The digital design flow has significant advantages of digital route availability, higher accuracy, simple tuning, low cost, predictability, less power consumption etc. (Ali et al., 2017). In ADPLL all these blocks are implemented in digital form and the signals connecting these blocks are also in digital form. Every block has its own role and function but if the major concern is power dissipation then electrically driven oscillator i.e. DCO is the most important component of ADPLL. The design of an electrically driven oscillator should always be adjusted, depending on the application. A DCO is characterized by its operating frequency range, maximum operational frequency and frequency resolution etc.

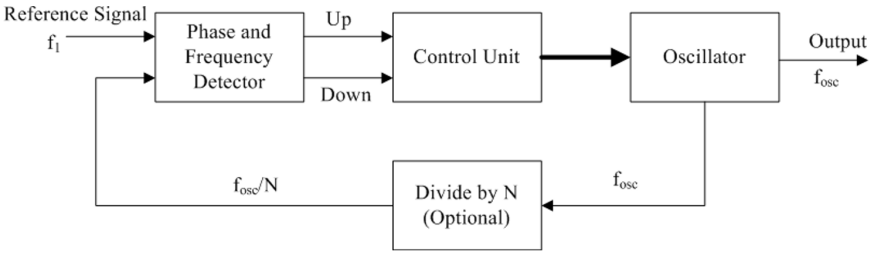

Figure 1: Basic block diagram of PLL.

The ADPLL mentioned in this study consists of four blocks namely Digital Phase Detector, Digital Loop Filter (DLF), Digital Controlled Oscillator (DCO) and Divide by N counter shown in Figure 2.(Kratyuk, Hanumolu, Moon, & Mayaram, 2007) It is controlled by a negative feedback closed loop, made up of digital chunks and only accepts digital signals. A bit signal or a group of bits signal i.e. word signal in electronic circuits could be used.

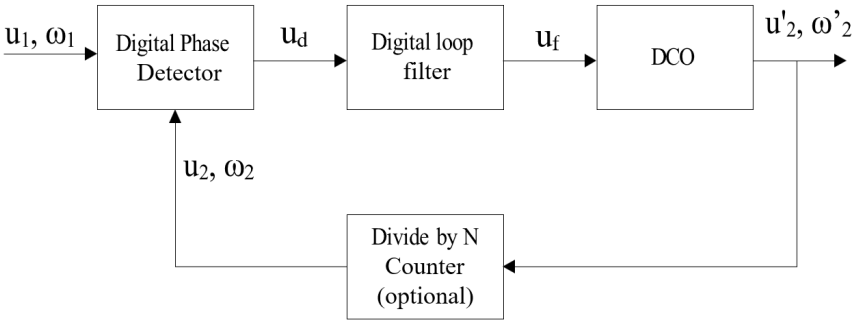

Figure 2: ADPLL Block Diagram.

It is made up of mainly four parts:

1. Digital Phase Detector (DPD): It generates an error signal between the two input signals it receives on the input. The digital loop filter has been chosen based on the advantages and disadvantages of various phase detectors.

2. Digital Loop Filter (DLF): It removes the high frequency components from the signal it receives at its input. DCO has been chosen based on the benefits and drawbacks of DLF.

3. Digitally Controlled Oscillator (DCO): By selecting the right DCO, the ripple problem has been eliminated, which is one of the most important parameters to consider while constructing an ADPLL.

4. Divide by N Counter: The fourth block frequency divider's purpose is to split the generating clock by programmable constants. The frequency divider's output has the matching frequency and amplitude as the reference clock when the PLL has been locked.

The ADPLL's goal is too formal to the event the phase inputs u_1 and u_2, as well as their frequency ω_1 and ω_2 respectively. DPD is used to minimize the disparity between these two signals namely reference signal and feedback signal and generates the error signal u_d. This u_d signal is either phase error or phase and frequency error signal. DLF is used to remove noise and generates the signal u_f which acts as input to the DCO. Finally, the signals from DLF are received by the digitally controlled oscillator (DCO), and generate output u'_2 with frequency ω'_2. This frequency can either similar or be higher than the reference signal in terms of frequency. If it is higher, then one additional block divide by N counter is used which divides the DCO generated output u'_2 by a factor N which is multiple of 2 and generates the signal u_2 with frequency ω_2. All existing block elements must be digital circuits to realize an ADPLL. For the power dissipation reduction the DCO block is very important and in the next section of the paper the commonly used oscillator architecture has been discussed.

3. Oscillator and Its Digital types

An oscillator is a closed loop circuit that generates a periodic output, without any input. The output is in the form of electrical signal of a particular frequency when the supply is turned ON. For the circuit to sustain its oscillation, Barkhausen's criteria should be satisfied. The Barkhausen's criteria state that around the loop total phase shift is said to be 360º which includes the 180º forward path phase shift and rest 180º phase shift is provided the feedback path and the overall gain of the circuit should be 1. For the oscillation to be build up the 360º phase shift is essential and overall unity gain of the loop helps to grow and then sustain the oscillation amplitude. In literature there are many types of oscillators exist for the analog circuit as well as digital circuits. Many types of oscillator are present in literature, the below explained two types of oscillators are considered to be an integral part of the PLL.

3.1. Ring Oscillator

Common source amplifier stage when placed in numerous numbers of stages forms the ring oscillator as shown in Figure 3. But when common source amplifier stage has been used as a distinct stage oscillator as shown in Figure 4, it does not oscillate the way it should be i.e. its oscillation does not grow or sustain. Therefore, single stage common source amplifier cannot be used as a ring oscillator until it has a phase shift of 360º.

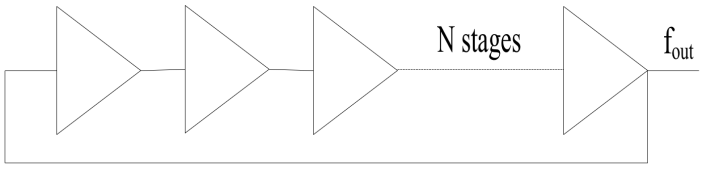

Figure 3: Ring Oscillator with N stages.

Hence, the odd number of stages of common source amplifier stage has been placed in the loop so that it acts as an oscillator. Therefore, it has been right to say that number of stages should be odd to act as a ring oscillator (Razavi, 2005). These odd number of stages i.e. N decides the ring oscillator frequency along with the each stage propagation delay t_p. The frequency of oscillation of ring oscillator is given by Eq.(1):

$$f = \frac{1}{2Nt_p} \tag{1}$$

They are generally used as data recovery and clock synchronization applications. It occupies the less area and it consumes less power compared to the other oscillators. The ring oscillator helps in to achieve wide tuning range. It has the disadvantage of very poor phase noise performance.

3.2. LC Oscillator

LC oscillator exhibits the good phase noise performance, hence, it is extensively chosen in the majority of the applications. This oscillator basically uses both inductor (L) and capacitor (C) in its circuit as revealed in Figure 5 which stores energy basically. When an initial condition is provided either to the inductor or

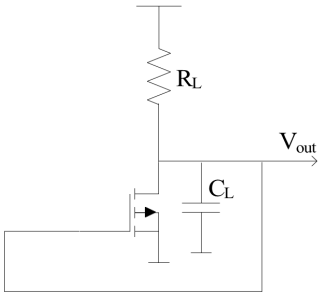

Figure 4: Common source amplifier stage.

the capacitor, oscillations take place. The inductor stores energy in the magnetic field when the current flows through it and the inductor gets charged, it starts discharging by storing its energy in the capacitor. When the discharging of inductor is complete the capacitor stores the energy in the voltage form between its plates. Now the discharging of the capacitor starts which charges the inductor, this process repeatedly occurs until the oscillation to die out due to the presence of internal resistance and this internal resistance loss is represented by R_p. In this manner the LC tank acts as an ideal resonator. For the compensation of this loss, a parallel negative resistance R_p is positioned; it helps in cancelling out the internal resistance of a resonant LC circuit and hence prevents the oscillation to die out.

The resonance of the LC oscillator takes place when the reactance of inductor X_L and capacitor X_C are opposite in sign and equal in magnitude. At that point their resonant frequency is represented by Eq. (2):

$$X_L = X_C \quad i.e. \quad \omega L = \frac{1}{\omega C}$$

$$f = \sqrt{\frac{1}{2\pi LC}} \tag{2}$$

where *C* - Capacitance, *L* - Inductance and ω - angular frequency.

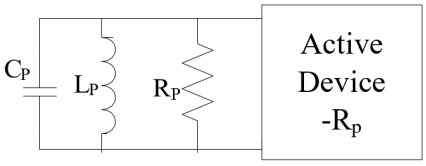

Figure 5: Basic circuit of LC oscillator.

where *L* - Reactance of inductor and *C* - Reactance of capacitor.

The main advantage of LC oscillator is good phase noise but has the disadvantage of large silicon area due to the presence of inductor and capacitor. In the oscillator designing, LC oscillator is preferred as the trade off between its advantage and disadvantage. In modern technology, CMOS oscillators are implemented either as LC oscillator or ring oscillator (Staszewski & Balsara, 2005).

4. Optimization Techniques

A lot of engineering applications, such as Internet of Things (IoT) and signal processing, require an efficient algorithm that can solve their optimization problems. In the field of engineering, optimization technique is a powerful tool to utilize the resources in a competent way as well as to decrease the environmental impact of a process. Application of optimization process helps us achieve the most favourable operating conditions. The primary goal of the optimization techniques is to minimize or maximize the objective function depending on the circumstances. Real world optimization problems have been solved by meta – heuristic algorithms including genetic algorithm (GA) and genetic programming and many more. Generally, most metaheuristic algorithms can solve many different types of optimizations problems.

A meta – heuristic algorithm is an optimization technique to find the solution of a complex problem which is difficult to solve for the optimality (Blum & Roli, 2003). In the world of limited resources, it is very important for finding the optimal solution with the incomplete information. Based on the operating search space metaheuristic algorithm is classified as nature inspired or non-nature inspired, physics or chemical based, population based or single point search etc. as shown in Table 1.

4.1. Levy Flight Algorithm

A collection of particles is used in this simple method at each "generation" stage. The program will produce a brand new generation at random distributed distances based on Levy flights, starting from one of the best known locations. The following step has been used to examine the new generation and choose the most promising one. The procedure is repeated until the halting requirements have been met (Hanert, 2012). It has been currently implemented in a rather straightforward manner. Only the finest option has been chosen.

4.2. Bat Algorithm

The only mammal that can fly is Bat. There are different kinds of bats and all kinds are of different sizes. Among its different varieties, microbats expansively use echolocation. Based on this echolocation, Bat Algorithm was firstly introduced by Yang (Yang, 2010a). They emit the short and loud pulse of sound and among them each sound burst last for few time. These sound strikes an object and after a few fraction of time echo returns to the ears of microbats. Based on that echo sound microbats are able to distinguish the difference between the prey and the obstacle, thus they are able to hunt in complete darkness (Chawla & Duhan, 2015; Y. Wang et al., 2019). This echolocation works as a type of sonar. This echolocation capability of microbats will be linked with the function to be optimized. Few assumptions made for Bat algorithm (Yang, 2010b) to solve the optimization problem are: to sense distance all bats use echolocation, they fly randomly at x_i position with v_i velocity in the fixed frequency range f_{min} to f_{max} , and loudness Ao in search of prey. Depending upon the closeness of the prey (target), the rate of emission of pulse i.e. r of bats can automatically be adjusted which is in the range 0 and 1. It is also supposed that bats loudness varies from a minimum constant value Amin to a large (positive) A_o. By adjusting the frequencies, pulse emission rates and their loudeness the new solutions are generated which in turn related to the appropriateness of the solution to the global optimal solution (Kumar & Bawa, 2019).

Table 1: Categorization of Meta – heuristic optimization Algorithms.

Bio- Stimulated Algorithms	**Evolutionary Algorithms**	**Nature – Inspired Algorithms**	**Swarm – Based Algorithms**	**Physics – based Algorithms**
Spotted Hyena Optimizer (SHO)	Differential Evolution (DE)	Invasive Weed Optimization (IWO)	Fish Swarm Algorithm (FSA)	Gravitational Search Algorithm (GSA)
Grey Wolf Optimizer (GWO)	Genetic Algorithm (GA)	Cuckoo Search Algorithm (CSA)	Particle Swarm Optimization (PSO)	Black Hole Algorithm (BHA)
Artificial Immune System (AIS)	Evolutionary Programming (EP)	Flower Pollination Algorithm (FPA)	Artificial Bee Colony (ABC)	Simulated Annealing (SA)
Dendritic Cell Algorithm (DCA)	Genetic Programming (GP)	BAT Algorithm (BA)	Ant Colony Optimization (ACO)	Harmony Search (HS)

4.3. Particle Swarm Optimization (PSO)

Each particle in the particle swarm optimization technique is comparatively autonomous and has two characteristics: velocity and position (Kennedy & Eberhart, 1995; D. Wang, Tan, & Liu, 2017; Ye et al., 2021). The direction of movement is represented by the position, while the pace of movement is represented by the velocity. Individually exploring the space, each particle looks for the best answer and logs it as the present extreme value. Particles discover the finest individual extreme value for the whole particle swarm and share their individual best position with it. The entire particle swarm shares the current global best position while each particle in the swarm adjusts its speed and location by the current individual best position. The most recent positions for each individual and the world will only change once per iteration. After the maximum number of iterations, the procedure comes to an end.

4.4. Ant Colony Optimization (ACO)

The ACO technique first produces several artificial ants and randomly distributes them to each coordinate. The artificial ants finish their various trips and choose the next city based on the probability function. The ants select the following city using the probability (also known as roulette) approach. In the upcoming tour, artificial ants' decision making is influenced by the pheromone concentration and the probability principle. Artificial ants scatter pheromones along the trail in a manner that resembles how ants forage. The pheromone only lasts for a brief while before dissipating. As a result, more pheromones are retained over the shorter route. Based on the pheromone concentration, other ants select a path. This favorable feedback makes them more likely to follow a route with a high pheromone concentration. For the ant colony optimization process, it is crucial to update the pheromones after completing a round trip and to evaporate the pheromones. Every tour's results will be updated after the maximum number of iterations has been reached (Dorigo & Caro, 1999).

Few of the metaheuristic algorithms have been explained above. The combination of two or more

metaheuristic optimization forms the hybrid optimization algorithm. These hybrid optimization algorithms have been used to obtain the better optimal solution. For the first time, these optimization algorithms have been proposed for obtaining the optimal solution of ADPLL's DCO parameter. In the next section, framework for parameter optimization has been discussed.

5. DCO Power Optimization

Now a days, for the portable battery operated device reduction in power consumption is the primary concern along with large battery time. In other words, it can be said that battery time has been increased by the reduction in the power consumption of the devices used in that system. Power saving has been the major concern for such application of ADPLL e.g. mobile, Internet of Things (IoT), digital signal processing of video applications and many more. As the ADPLL has the four key blocks namely phase detector, loop filter, oscillator and divide by N counter. The DCO in the ADPLL contributes to more than 50 % of the total power consumption. Thus, it will be right to say that power reduction in ADPLL is significantly reduced by reducing the DCO power consumption. The DCO in the ADPLL dictates the frequency range, maximum frequency of the ADPLL. For the word signals, the main criterion for the DCO designing is to provide the acceptable jitter and enough control word resolution. The nature inspired algorithms are based on the population of species. Each individual represents a search point in the feasible solution space which is exposed to learning process. Initially the population and its parameters are initialized randomly and then subject to the process of selection through several individuals such that the parameter updation of each individual evolve towards more favourable regions of the search space. By evaluating the fitness of each among all the individuals in the population the progress in the search is achieved, then selection of the individual with a better fitness value and then comparing them with the others and then again evaluating it. After a few iterations, the program converges and the best individual represents the optimum solution. There are several nature inspired algorithms, but their basic structure is the same (Reddy & Kumar, 2012). The framework of the DCO parameter optimization using nature inspired algorithm is shown in Figure 6.

Different architectures of DCO have been available in literature. In the research, for the optimization algorithm to work a specific architecture has been chose in which DCO in which it is implemented in two stages i.e. coarse tuning block and fine tuning block. The objective function is minimization of power consumption and constraints have been described according to the optimization algorithm and architecture of the DCO considered. For the nature inspired optimization algorithms, to obtain optimal DCO parameters general algorithm steps have been described below:

1. Initialize the population and its parameters using random generation
2. Calculate the initial solution for initial positions using objective function
3. For each individual in the population evaluate the fitness and select the initial best solution for best fitness value
4. Until stopping criterion satisfied, repeat the evaluation steps:

(a) Update the parameters of each individual

(b) Select the best solution among them

(c) Calculate the objective function

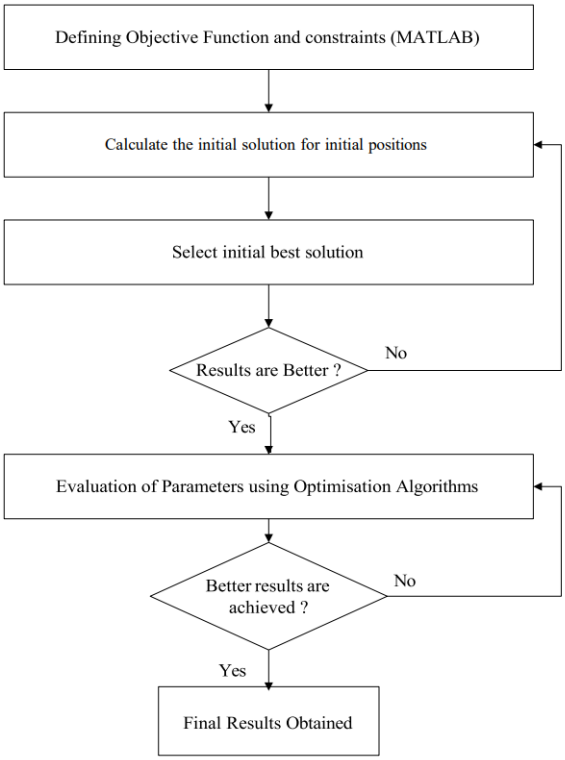

Figure 6: Framework for DCO parameter optimization.

5. The fittest individual has been reported as the best solution.

Using above mentioned steps meta – heuristic algorithms will be used to obtain the optimal solution of the two stage DCO parameters and the objective function which when designed reduces the power consumption leads to overall reduction in the power consumption of the ADPLL.

6. Conclusion and Future Work

ADPLL is a negative feedback closed loop circuit to match the phase and frequency of the two signals. It found its application in the various fields like mobile phones, communication system, signal processing, biomedical instruments and IoT. As the technology progresses, the handling of the portable device have been increased which demands the long battery life. It is possible only when the circuits used in the devices consume the less power. For the power reduction in the circuits, different techniques are available either at the transistor level designing or at the block level. In ADPLL, DCO consumes more than half of the overall power consumption. In this paper, first time a framework is suggested for the power reduction in DCO using nature inspired algorithms. The nature inspired algorithms have been used to obtain the optimal solution of a given problem either by minimizing or maximizing the objective function. In future, the suggested framework will be implemented to obtain optimal solution for the parameters by minimizing the overall power consumption objective and then using that optimal solution DCO will be designed.

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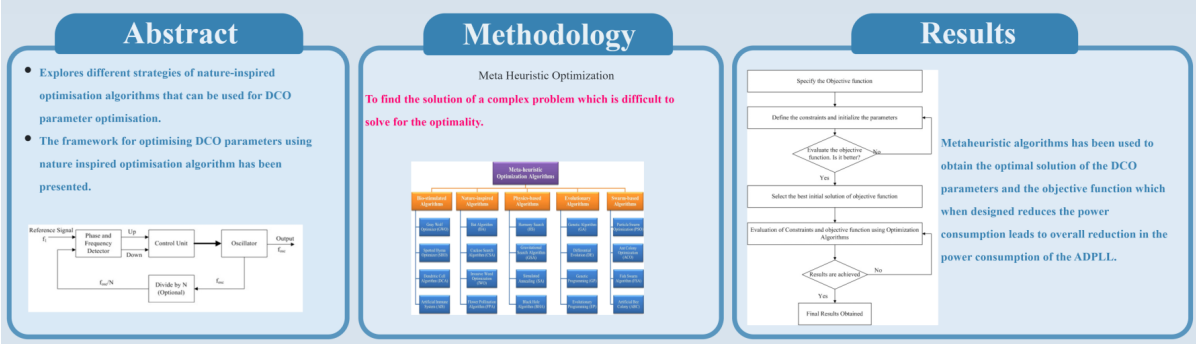
Graphical Abstract



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